WHAT IS CLAIMED IS:

1. A memory array circuit comprising:

memory cells;

first read bit lines coupled to a first subset of the memory cells; and

first NAND gates coupled to the first read bit lines, wherein each of the first NAND gates has two inputs that are coupled to two of the first read bit lines.

2. The memory array according to claim 1 further comprising:

first transistors, each of the first transistors having an input coupled to an output of one of the first NAND gates; and

a first global bit line coupled to each of the first transistors.

3. The memory array according to claim 2 further comprising:

a second pull up transistor coupled to the first global bit line; and

third pull up transistors, wherein each of the third pull up transistors are coupled to one of the first read bit lines, and the first transistors are pull down transistors.

4. The memory array according to claim 2 further comprising:

second read bit lines coupled to a second subset of the memory cells; and

second NAND gates coupled to the second read bit lines, wherein each of the second NAND gates has two inputs that are coupled to two of the second read bit lines.

5. The memory array according to claim 4 further comprising:

second transistors, each of the second transistors having an input coupled to an output of one of the second NAND gates; and

a second global bit line coupled to each of the second transistors.

6. The memory array according to claim 5 further comprising:

a third NAND gate having a first input coupled to the first global bit line and a second input coupled to the second global bit line.

7. The memory array according to claim 5 further comprising:

a repeater circuit coupled between the first global bit line and the second global bit line.

8. The memory array according to claim 7 wherein:

the repeater circuit includes an inverter coupled to a third transistor.

9. A memory array circuit comprising:

memory cells;

first local read bit lines coupled to a first subset of the memory cells;

first logic gates, each coupled to receive signals on two of the first local read bit lines;

a first global bit line; and

first transistors coupled between the first global bit line and the first logic gates.

10. The memory array circuit according to claim 9 further comprising:

second local read bit lines coupled to a second subset of the memory cells;

second logic gates, each coupled to receive signals on two of the second local bit lines;

a second global bit line; and

second transistors coupled between the second global bit line and the second logic gates.

11. The memory array according to claim 10 further comprising:

an inverter circuit coupled to the first global bit line; and

a third transistor coupled to the inverter circuit and the second global bit line.

12. The memory array according to claim 10 wherein:

the first logic gates and the second logic gates are NAND gates.

13. The memory array according to claim 10 further comprising:

a NAND gate having a first input coupled to the first global bit line and a second input coupled to the second global bit line.

14. The memory array circuit according to claim 9 further comprising:

a first pre-charge transistor coupled to the first global bit line; and

a plurality of second pre-charge transistors that are each coupled to one of the first local read bit lines.

15. A method for reading bits from memory cells in a memory array, the method comprising:

accessing a first bit from a first memory cell on a first local read bit line;

transmitting a signal indicative of the first bit from the first local read bit line to a first global bit line through a first logic gate;

accessing a second bit from a second memory cell on a second local read bit line; and

transmitting a signal indicative of the second bit from the second local read bit line to the first global bit line through the first logic gate.

16. The method according to claim 15 wherein:

the first logic gate is a NAND gate.

17. The method according to claim 15 wherein transmitting the signals indicative of the first and the second bits further comprises:

transmitting the signals indicative of the first and the second bits from the first logic gate to a transistor that is coupled to the first global bit line.

18. The method according to claim 15 further comprising:

accessing a third bit from a third memory cell on a third local read bit line;

transmitting a signal indicative of the third bit from the third local read bit line to the first global bit line through a second logic gate;

accessing a fourth bit from a fourth memory cell on a fourth local read bit line; and

transmitting a signal indicative of the fourth bit from the fourth local read bit line to the first global bit line through the second logic gate.

19. The method according to claim 15 further comprising:

accessing a third bit from a third memory cell on a third local read bit line;

transmitting a signal indicative of the third bit from the third local read bit line to a second global bit line through a second logic gate;

accessing a fourth bit from a fourth memory cell on a fourth local read bit line; and

transmitting a signal indicative of the fourth bit from the fourth local read bit line to the second global bit line through the second logic gate.

20. The method according to claim 19 further comprising:

transmitting the signal indicative of the first bit from the first global bit line to the second global bit line through a repeater circuit.

21. The method according to claim 20 wherein the repeater circuit comprises an inverter coupled to the gate of a field effect transistor, and the field effect transistor pulls down the voltage on the second global bit line.

22. The method according to claim 19 wherein:

the first and the second logic gates are NAND gates.

23. The method according to claim 19 further comprising:

transmitting a signal indicative of the first bit or the second bit from the first global bit line to a third level bit line through a NAND gate; and

transmitting a signal indicative of the third bit or the fourth bit from the second global bit line to the third level bit line through the NAND gate.